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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,395	07/16/2003	Yibing Zhao	Analog.7042	9544

7590 11/24/2004

Attn: Matthew E. Connors
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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,395	ZHAO ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-17 and 22-34* is/are allowed.

6)☒ Claim(s) *1,2,4-7,18 and 35-37* is/are rejected.

7)☒ Claim(s) *3,19-21,38 and 41-44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/16/03 & 3/18/04*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 7, 35-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Kameyama et al (5,748,053).

Claim 1, Kameyama shows a switch (Fig. 14) comprising: a plurality of field effect transistors (712-713) connected in series, each field effect transistor including a gate, a source, and a drain; said gate of one of said series connected field effect transistors being a different size (1mm) from said gate of another series connected field effect transistor (0.4mm).

Claim 2, Kameyama shows wherein said gate of one of said plurality of series connected field effect transistor has a longer gate length and/or gate width (1mm/0.4mm) than said gate of said other series connected field effect transistor.

Claim 7, Kameyama shows the different gate sizes increase a parasitic capacitance within the switch.

Claim 35, Kameyama shows a radio frequency single pole double throw switch (Fig. 14), comprising: a receiver port (703); a transmitter port (702); an antenna port (701); a receiver section connecting said receiver port to said antenna; and a transmitter section connecting said transmitter port to said antenna; said receiver section including

a plurality of field effect transistors (712-713) connected in series, each field effect transistor including a gate, a source, and a drain such that one of said series connected field effect transistors has a modified gate therein that is a different size (1mm) from said gate of another series connected field effect transistor (0.4mm).

Claim 36, Kameyama shows wherein the source of said modified gate transistor is connected to said receiver port.

Claim 37, Kameyama shows wherein the drain of said modified gate transistor is connected to said antenna port.

Claim 40, Kameyama shows wherein said gate of one of said plurality of series connected field effect transistor has a longer gate length and/or gate width (1mm/0.4mm) than said gate of said other series connected field effect transistor.

Claim 45, Kameyama shows the different gate sizes increase a parasitic capacitance within the switch.

Claim 46, Kameyama shows the different gate sizes improve the linearity without impacting the ESD and EOS ruggedness.

3. Claims 1-2, 4-6, 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al (EP 0,700,161).

Claim 1, Tanaka shows a switch (Fig. 1) comprising: a plurality of field effect transistors (FET2-2, FET2-1, FET3) connected in series, each field effect transistor including a gate, a source, and a drain; said gate of one of said series connected field

effect transistors being a different size (1mm) from said gate of another series connected field effect transistor (gates FET2-1 is different from gate FET3).

Claim 2, Tanaka shows wherein said gate of one of said plurality of series connected field effect transistor has a longer gate length and/or gate width (a large gate, page 7, line 42) than said gate of said other series connected field effect transistor.

Claim 4, Tanaka shows the gate of one of the plurality of series connected field effect transistor has a distance to its source port that is less than a distance to its drain port (Fig. 11).

Claims 5-6, Tanaka shows the gate of the other series connected field effect transistor (FET3) has a distance to its source port that is equal to a distance to its drain port (inherent limitation since there is no modification of transistor FET3).

Claim 18, Tanaka shows A high-electron-mobility-transistor (Fig. 10), comprising: two gate fingers (G1, G2); a transistor connection segment between said gate fingers; and a heavily doped cap layer fabricated (D1, D2) upon said transistor connection segment between said gate fingers.

Allowable Subject Matter

4. Claims 3, 19-21, 38, 41-44 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 8-17, 22-34 are allowed.

6. The following is an examiner's statement of reasons for allowance: series connected dual-gate transistor having different size.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anh Q. Tran
Examiner
Art Unit 2819

ANH Q. TRAN
PRIMARY EXAMINER

11/18/04